WHAT IS CLAIMED IS

1. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by a plasma CVD process, with a high-frequency power set smaller than a high-frequency power in which said first insulation film contains H_2O with an amount of about 2.4 wt%.

2. A method as claimed in claim 1, wherein said high-frequency power is set smaller than a high-frequency power in which said first insulation film contains H_2O with an about of about 1.1 wt% or less.

3. A method as claimed in claim 1, wherein said high-frequency power is set smaller than about 100 W.

4. A method as claimed in claim 1, wherein said high-frequency power is set between about 50 W and about 100 W.

5. A method as claimed in claim 1, wherein said first insulation film has a refractive index of about 1.5.

6. A method as claimed in claim 1, wherein said plasma CVD process is conducted while using SiH_4 and N_2O as source materials, with a proportion of N_2O with respect to SiH_4 set to be about 10 or less.

7. A method as claimed in claim 1, further including a step, after said step of forming said first insulation film and before said step of forming said second insulation film, of annealing said first insulation film.

8. A method as claimed in claim 7, wherein said annealing step is conducted by a rapid heating process.

9. A method as claimed in claim 1, wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

10. A method as claimed in claim 1, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of

said diffusion region, and wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

11. A method as claimed in claim 1, further comprising a step, before said step of forming said first insulation layer, of forming a conductor pattern in contact with said diffusion region.

12. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by a CVD process that uses SiH_4 and N_2O as source gases.

13. A method as claimed in claim 12, wherein said CVD process is conducted while setting a ratio of N_2O with respect to SiH_4 to about 5 or less.

14. A method as claimed in claim 12, wherein said CVD process is conducted at a substrate temperature of about 825°C or less.

15. A method as claimed in claim 12, further including a step, after said step of forming said first insulation film and before said step of

forming said second insulation film, of annealing said first insulation film.

16. A method as claimed in claim 12, wherein said annealing step is conducted by a rapid heating process.

17. A method as claimed in claim 12, wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

18. A method as claimed in claim 12, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of said diffusion region, and wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

19. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate

adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by depositing a silicate glass containing P.

20. A method as claimed in claim 19, wherein said silicate glass contains P therein with an amount of about 6 wt% or less.

21. A method as claimed in claim 19, wherein said silicate glass further contains B.

22. A method as claimed in claim 21, wherein said silicate glass contains B with an amount of about 4 wt% or less.

23. A method as claimed in claim 19, further including a step, after said step of forming said first insulation film and before said step of forming said second insulation film, of annealing said first insulation film.

24. A method as claimed in claim 23, wherein said annealing step is conducted by a rapid heating process.

25. A method as claimed in claim 19,

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wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

26. A method as claimed in claim 19, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of said diffusion region, and wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

27. A method as claimed in claim 19, further comprising a step, before said step of forming said first insulation layer, of forming a conductor pattern in contact with said diffusion region.

28. A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode; and

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region;

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film contains H_2O with an amount smaller than about 2.4 wt%.

29. A semiconductor device as claimed in claim 28, wherein said first insulation film contains H_2O with an amount of about 1.1 wt% or less.

30. A semiconductor device as claimed in claim 28, wherein said first insulation film is an oxide film having a refractive index of about 1.5.

31. A semiconductor device as claimed in claim 28, further comprising a conductor pattern

contacting with said diffusion region and said gate electrode such that said conductor pattern extends between said side wall oxide film and said first insulation film along a surface of said side wall oxide film.

32. A semiconductor device as claimed in claim 28, further comprising a silicide layer on a surface of said diffusion region.

33. A semiconductor device as claimed in claim 32, further comprising a silicide layer on a surface of said gate electrode.

34. A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode; and

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region;

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide

film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of PSG containing P with an amount of about 6 wt% or less.

35. A semiconductor device as claimed in claim 34, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends between said side wall oxide film and said first insulation film along a surface of said side wall oxide film.

36. A semiconductor device as claimed in claim 34, further comprising a silicide layer on a surface of said diffusion region.

37. A semiconductor device as claimed in claim 36, further comprising a silicide layer on a

surface of said gate electrode.

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39. A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode; and

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region;

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of BPSG containing B with an amount of about 4 wt% or less.

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40. A semiconductor device as claimed in

claim 39, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends between said side wall oxide film and said first insulation film along a surface of said side wall oxide film.

41. A semiconductor device as claimed in claim 39, further comprising a silicide layer on a surface of said diffusion region.

42. A semiconductor device as claimed in claim 41, further comprising a silicide layer on a surface of said gate electrode.